Universidad de Alcalá

TEACHING GUIDE

Digital Electronics

Degree in
Telecommunication Technologies Engineering (GITT)
Telecommunication Systems Engineering (GIST)
Telematics Engineering (GIT)
Electronic Communications Engineering (GIEC)

Universidad de Alcalá

Academic Year 2023/2024

2nd Year - 2nd Semester (GITT+GIST+GIT+GIEC)

Approved by the School Board on June 12th, 2023

TEACHING GUIDE

Course Name:	**Digital Electronics**
Code:	**350007 (GITT+GIST+GIT+GIEC)**
Degree in:	**Telecommunication Technologies Engineering (GITT)** **Telecommunication Systems Engineering (GIST)** **Telematics Engineering (GIT)** **Electronic Communications Engineering (GIEC)**
Department and area:	**Electrónica** **Electronic Technology**
Type:	**Compulsory (GITT+GIST+GIT+GIEC)**
ECTS Credits:	**6.0**
Year and semester:	**2nd Year - 2nd Semester (GITT+GIST+GIT+GIEC)**
Teachers:	View website https://portal.uah.es/epd2_asignaturas/asig350007
Tutoring schedule:	View website
Language:	English

1. COURSE SUMMARY

The aim of this course is to introduce students to the study and basic design of digital systems, both combinational and sequential. Hardware Description Languages â€‹â€‹(HDL) and Programmable Logic Devices (PLD) are presented. On this basis, it is possible to address systems based on microprocessors, microcontrollers, system-specific hardware, etc. that will be discussed in subsequence subjects.

It will be necessary to have prior knowledge acquired in the course of Circuit Analysis and Fundamentals of Electronics. It is particularly interesting to have attended and passed lab part of this subject. Knowledge of Boolean Algebra, acquired in Linear Algebra, is also required.

The knowledge acquired in this subject is necessary in any other that partially includes digital electronic circuits. However, the subjects with a direct dependency of Digital Electronics are Digital Electronic Systems, Advanced Digital Electronic Systems (GIEC, GITT) and Electronic Design (GIEC, GITT).

2. SKILLS

Basic, Generic and Cross Curricular Skills.

This course contributes to acquire the following generic skills, which are defined in the Section 3 of the Annex to the Orden CIN/352/2009:

en_TR2 - Knowledge of basic subjects and technologies that enables to learn new methods and technologies, as well as to provide versatility that allows adaptation to new situations.

en_TR8 - Capacity of working in a multidisciplinary and multilingual team and of communicating, both in spoken and written language, knowledge, procedures, results and ideas related to telecommunications and electronics.

Professional Skills

This course contributes to acquire the following professional skills, which are defined in the Section 5 of the Annex to the Orden CIN/352/2009:

en_CT1 - Skills for autonomous learning of new concepts and techniques suitable for the conception, development or commissioning of telecommunication systems and services.

en_CT3 - Ability to use computer tools to search bibliographic resources or information relating to telecommunications and electronics.

en_CT9 - Ability to analyze and design combinational and sequential circuits, synchronous and asynchronous, and (partially) use of microprocessors and integrated circuits.

en_CT10 - Knowledge and application of the principles of Hardware Description Languages.

Learning Outcomes

RA1. Apply the properties of the logic functions that describe a digital system to the implementation with logic gates.

RA2. Identify and use correctly the different combinational circuits present in digital systems, including the basic binary-arithmetic ones.

RA3. Identify and use correctly the sequential circuits present in digital systems.

RA4. Analyze digital systems including combinational and/or sequential blocks.

RA5. design digital systems including combinational and/or sequential blocks.

RA6. Apply the Mealy and Moore finite-automata methodology to the design of synchronous sequential systems.

RA7. Transfer all the topics addressed in previous points to real circuit implementation.

3. CONTENTS

Contents Blocks	Total class hours (L / Prob / Lab)
Introduction. Overview of digital circuits. Boolean algebra. Basic logic gates. Synthesis and implementation of logic functions. Basics of logic families: voltage levels, currents and compatibility. Propagation time. Tristate gates. Introduction to programmable logic devices and VHDL	8 / 3 / 0
Analysis and design of combinational digital circuits: multiplexers, demultiplexers, decoders and drivers (BCD-7s), encoders, comparators and binary arithmetic circuits.	6 / 4 / 10
Analysis and design of sequential digital circuits: bistables, registers and counters.	5 / 4 / 8
Synthesis of sequential systems. Sequential systems design: Moore and Mealy automata.	4 / 4 / 0

These contents add up to 56 hours of lectures, problems and lab and, coupled to two-hour mid-term tests and two hours of final evaluation, make 58 hours in a classroom setting.

Students are also provided, on the course website (UAH virtual platform: http://www.uah.es/aula_virtual), with a detailed description that includes:

- Contents of in-person classes.
- Available resources for each lesson.
- Work that the students must perform before and after classes in the hours allotted for their work.

4. TEACHING - LEARNING METHODOLOGIES. FORMATIVE ACTIVITIES.

4.1. Credits Distribution

Number of on-site hours:	58 hours (56 hours on-site +2 exams hours)
Number of hours of student work:	92
Total hours	150

4.2. Methodological strategies, teaching materials and resources

In the teaching-learning process the following training activities will be held:

- Lectures (theory classes) given in large groups based on presentations that allow the teacher to introduce the skills necessary for the proper development of the learning process. These classes will present essential contents, subject of a reasoned conceptual learning, subsequently used to develop broader skills.
- Practical classes taught in large groups based mainly on solving exercises and problems. The aim of these classes is to promote meaningful learning that will allow students to deepen the knowledge acquired, relate and apply it creatively in order to solve situations, as the course progresses, that will gradually become more similar to real-world engineering problems.
- Lab classes taught exclusively in small groups and based on practical circuit implementation, scheduled so that they serve as a complement for better understanding of the concepts acquired in the room sessions, through practical experimentation.
- Tutorship sessions: individual or group sessions.

The following additional resources may also be used:

- Individual and group works, which could pose, in addition to its realization, the relevant public presentation to the rest of the class to stimulate discussion.
- Attendance at conferences, meetings or discussions related scientific field.

In the lab classes, the students will have at their disposal a work station provided with the basic equipment (oscilloscope, power supply end signal generator) and a computer with HDL design and simulation software.

Throughout the learning process in the course, students will use different bibliographic and electronic resources, in order to become familiar with the environments of documentation they will use professionally in the future. In addition, teachers will provide own materials developed specifically for the course (theoretical papers, collections of exercises and problems, practice manuals, audio visuals, etc.) so that students can meet the course objectives and achieve the skills described.

Students will be provided throughout the semester with tutorship in group (if requested by the students themselves) or individual. Whether individually or in small groups, this tutorship will resolve doubts and consolidate the knowledge acquired. Also it will help to make appropriate monitoring and assess the proper functioning of the mechanisms of teaching and learning.

Finally, the whole development of the subject will be detailed on the website of the course (UAH virtual platform). All resources developed for the subject, such as slides, exercise statements and solutions, statements of problems for practices, detailed schedules for each group and class, mid-term exam mark and any other information that teachers consider appropriate for the proper teaching and learning process will be available on the website.

5. ASSESSMENT: procedures, evaluation and grading criteria

Preferably, students will be offered a continuous assessment model that has characteristics of formative assessment in a way that serves as feedback in the teaching-learning process.

5.1. PROCEDURES

The evaluation must be inspired by the criteria of continuous evaluation (Regulations for the Regulation of Teaching Learning Processes, NRPEA, art 3). However, in compliance with the regulations of the University of Alcalá, an alternative process of final evaluation is made available to the student in

accordance with the Regulations for the Evaluation of Apprenticeships (approved by the Governing Council on March 24, 2011 and modified in the Board of Directors). Government of May 5, 2016) as indicated in Article 10, students will have a period of fifteen days from the start of the course to request in writing to the Director of the Polytechnic School their intention to take the non-continuous evaluation model adducing the reasons that they deem convenient. The evaluation of the learning process of all students who do not apply for it or are denied it will be done, by default, according to the continuous assessment model. The student has two calls to pass the subject, one ordinary and one extraordinary.

According to current UAH regulations, and, as long as the laboratory module is considered as an essential part to reach the capacities aimed by the Digital Electronics course, attendance to all the lab practicals, as well as successfully completing them, is considered as an essential and also compulsory element for the course assessment, either under continuous assessment or final evaluation format. For this reason, lab practicals are common and mandatory, both for continuous and final assessment too.

5.2. EVALUATION

EVALUATION CRITERIA

After having completed the course, the student should be able to:

CE1. Solve basic problems related to the basics of combinational logic.

CE2. Correctly analyze and synthetize digital subsystems integrated by different combinational blocks.

CE3. Analyze and synthetize digital systems including both combinational and sequential blocks.

CE4. Propose simple and simplified solutions to the problems solved.

CE5. Provide a correct, accurate and concise explanation to the solution proposed for a problem or for a lab practical design.

CE6. Propose a design, and implement a practical solution, to solve a certain problem statement (either guided or unguided).

CE7. Make previous work before practical sessions, necessary to make good use of them, including reading the subject documentation, understanding technical information, studying the theoretical background, solving the problems related to the session and having the necessary materials.

CE8. Produce correct technical reports and make a structured and clear presentation (if required) of the work carried out.

GRADING TOOLS

The following assessment tools will be used:

- **PEI:** A first mid-term tests, which will consist of several questions of analysis and / or synthesis referred to the content of the syllabus taught up to the date of this test.
- **PEIR:** Mid-term test recovery exam.
- **PEF:** Final exam, with several questions of analysis and / or synthesis, referred to the contents of the content of the syllabus covered by the theory and exercises classes.
- **PL:** Four lab projects covering the whole subject knowledge including combinational and sequential circuits. They are continuously assessed along the practical sessions.

MARKING CRITERIA

The following table relates skills, learning results and assessment criteria with the assessment tools and the specific percentages assigned.

Continuous assessment, ordinary exam.

Skill	Learning Outcomes	Evaluation criteria	Grading Tool	Contribution to the final mark
TR2, TR8, CT1, CT3, CT9	RA1,RA2	CE1, CE2, CE4, CE5CE1, CE2, CE4, CE5	PEI/PEIR	35%
TR2, TR8, CT1, CT3, CT9	RA1-RA6	CE1-CE5	PEF	35%
TR2, TR8, CT1, CT3, CT9, CT10	RA7	CE4-CE8	PL	30%

A student will successfully pass the course following the continuous assessment model if he or she shows that has acquired the theoretical and practical skills, which means:

- The student has done the mid-term test.
- The student have satisfactorily passed the evaluation of skills related to laboratory projects. It will be understood that a student acquires these skills satisfactorily, if he attends the laboratory and he has obtained a mark equal or greater than the 45% of the maximum possible total mark in the set of laboratory practices.
- The student has obtained a mark equal or greater than the 45% of the maximum possible total mark in the theory-tests carried out (hence successfully passing the evaluation of the skills and skills related to theory tests).
- The student must obtain a final global mark equal to or greater than 5 (out of 10) calculated as a weighted average with the percentages detailed before.

The student will have the option to perform a recovery exam, PEIR, of the contents evaluated in the PEI, to be done on the same day as the final exam. The qualification of these contents will be the highest of the scores obtained in the PEI and the PEIR.

The student who follows the continuous assessment process is considered as presented, in case he performs, apart from the laboratory practicals, the PEF test.

In case the student does not successfully pass the assessment of the skills related to the set of all tests, the final mark will be the lower of the following:

- The weighted sum of all marks.
- 4,0 out of 10 points.

Final assessment, ordinary and extraordinary exams.

The final assessment, both in ordinary and extraordinary exams, are ruled by the following directions:

Skill	Learning Outcomes	Evaluation criteria	Grading Tool	Contribution to the final mark
TR2, TR8, CT1, CT3, CT9	RA1-RA6	CE1-CE5	PEF	70%
TR2, TR8, CT1, CT3, CT9, CT10	RA7	CE4-CE8	PL	30%

In order to pass the course, either in the ordinary or in extraordinary exam, the student must show that he/she has successfully acquired the practical skills corresponding to the lab sessions (i.e., he/she has attended and carried out all the scheduled regular lab practicals, as explained in previous sections), and has obtained a mark equal or greater than the 45% of the maximum possible total mark in the theory-tests carried out (hence successfully passing the evaluation of the skills related to theory tests). The final global mark must be equal to or grater than 5 (out of 10) calculated as a weighted average with the

corresponding percentages detailed for the extra exam session.

In the extraordinary exam, those students that having attended the laboratory, want to improve the qualification obtained in the projects, will be able to take a specific, face-to-face, individual and practical test, which will be carried out in the laboratory, upon request.

6. BIBLIOGRAPHY

6.1. Basic Bibliography

- Course notes specifically prepared by teachers which will be provided to students directly through the website of the course (including slides, notes, data sheets and collections of exercises).
- Digital Fundamentals. Thomas L. Floyd. Prentice Hall. Comprehensive and detailed introduction to digital electronics covering all aspects of the syllabus except the design of synchronous sequential circuits. It is especially interesting because of the number of solved examples and exercises.
- Websites on the topic of the course to be selected in advance by the faculty.

6.2. Additional Bibliography

- Digital Systems. Principles and Applications. Ronald. J. Tocci. Prentice Hall. It is also a book with a broad introduction to digital electronics that fits quite well the basic concepts of this course.
- The VHDL cookbook. Peter J. Ashenden. Dept. Computer Science, University of Adelaide, South Australia
- Diseño de Sistemas Digitales con VHDL. S. Alonso, E. Soto y S. Fernández. Ed. Thomson, 2002.
- RTL hardware design using VHDL: coding for efficiency, portability,and scalability (2006). Pong P. Chu. Ed. John Wiley & Sons Inc.

Disclosure Note

During the evaluation tests, the guidelines set out in the Regulations establishing the Rules of Coexistence of the University of Alcalá must be followed, as well as the possible implications of the irregularities committed during said tests, including the consequences for committing academic fraud according to the Regulation of Disciplinary Regime of the Students of the University of Alcalá.