Universidad de Alcalá

TEACHING GUIDE

Electronic Design

Degree in
Telecommunication Technologies Engineering

Universidad de Alcalá

Academic Year 2024/2025

3rd Year - 1st Semester

Approved by the EPS School Board on June 14th, 2024

TEACHING GUIDE

Course Name:	**Electronic Design**
Code:	**350021**
Degree in:	**Telecommunication Technologies Engineering**
Department and area:	**Electrónica** **Electronic Technology**
Type:	**Compulsory**
ECTS Credits:	**6.0**
Year and semester:	**3rd Year, 1st Semester**
Teachers:	Álvaro Hernandez Alonso Pablo Ramos Sainz Carlos Cruz de la Torre
Tutoring schedule:	Visit the UAH website
Language:	Spanish/English friendly

1. COURSE SUMMARY

The main goal of the Electronic Design course is the study of the methodologies and tools for design and verification of digital and analog electronic systems. Contents will be specially focused on the design of digital subsystems on programmable devices.

This course requires previous aspects and contents already studied in the following courses: Digital Electronics and Circuit Electronics.

2. SKILLS

Basic, Generic and Cross Curricular Skills.

This course contributes to acquire the following generic skills, which are defined in the Section 3 of the Annex to the Orden CIN/352/2009:

en_TR2 - Knowledge of basic subjects and technologies that enables to learn new methods and technologies, as well as to provide versatility that allows adaptation to new situations.

en_TR8 - Capacity of working in a multidisciplinary and multilingual team and of communicating, both in spoken and written language, knowledge, procedures, results and ideas related to telecommunications and electronics.

Professional Skills

This course contributes to acquire the following professional skills, which are defined in the Section 5 of the Annex to the Orden CIN/352/2009:

en_CSE1 - Ability to build, operate and manage capture, transportation, representation, processing, storage, management and presentation of multimedia information systems, from the point of view of the electronic systems.

en_CSE2 - Ability to select circuits and electronic devices specialized for transmission, routing and terminals, both in fixed and mobile environments.

en_CSE3 - Ability to perform the specification, implementation, documentation and tuning of equipment and systems, electronic, instrumentation and control, considering both the technical aspects and the corresponding regulatory regulations.

en_CSE5 - Ability to design analog and digital electronic circuits, analog-digital and digital-analogue conversion, radio frequency, power and conversion of electric power for applications of telecommunication and computing.

en_CSE7 - Ability to design interface devices, data capture and storage, and terminals for telecommunication services and systems.

Learning Outcomes

The expected learning outcomes, expressed in the form of knowledge and skills and abilities that students should have achieved are as follows:

RA1. Knowledge of technological alternatives for the design of analog and digital electronic systems, focusing on programmable logic devices.

RA2. Apply design and verification methodologies in digital electronic circuits.

RA3. Manage hardware description languages in the design and verification of electronic circuits.

RA4. Design advanced architectures for combinational and sequential systems: arithmetic blocks, pipelining, and timing analysis.

RA5. Calculate and design analog circuits.

RA6. Identify testing techniques in electronic circuits and capability to apply those techniques.

RA7. Describe most significant microelectronic technologies.

3. CONTENTS

Content modules	Hours
Course introduction	1 hour
Chapter 1. Technological alternatives for the design of electronic systems.	3 hours
Chapter 2. Hardware description language.	24 hours (12 GG + 12 GP)
Chapter 3. Design of digital subsystems.	16 hours (4 GG + 12 GP)
Chapter 4. Design of analog subsystems.	2 hours
Chapter 5. Test for integrated circuits.	4 hours
Chapter 6. Microelectronic Technology.	4 hours

These contents imply 54 hours of lectures, dedicated to theory, exercises and lab, which, together with two hours from an intermediate assessment and other two hours from a final test, provide 58 hours in lectures for the course.

Note: GG= Large group (theory and exercises); GP=Small group (lab practices).

4. TEACHING - LEARNING METHODOLOGIES. FORMATIVE ACTIVITIES.

4.1. Credits Distribution

Number of on-site hours:	58 hours (54 hours on-site + 2 hours for intermediate assessment + 2 hours for final assessment)
Number of hours of student work:	92
Total hours	150

4.2. Methodological strategies, teaching materials and resources

The teaching-learning process will be carried out through the following activities:

- Theory classes and practical lectures for exercises.

- Practical laboratory classes.
- Tutorials: individual and group.

The following additional resources could also be used, among others:

- Individual and group work, including proposed problem solving, with the additional possibility of making a public presentation to the rest of the students to foster discussion and improve the assimilation of key concepts.
- Attendance at conferences, meetings and scientific discussions related to the course topics.

Throughout the course, theoretical and practical activities will be proposed to the students. Practical work will be carried out in the laboratory to complement and support the teaching of theoretical concepts, or develop additional skills. In this way the student can experiment and thus consolidate the acquired concepts, both individually and in groups.

For the laboratory assignment, the student will have access to basic equipment (oscilloscope, power supply, signal generator) and a computer with electronic circuit design and simulation software.

Along the course, students should make use of different sources and electronic or bibliographic resources, so that they will become acquainted with the future documentation environments they will use professionally.

5. ASSESSMENT: procedures, evaluation and grading criteria

Preferably, students will be offered a continuous assessment model that has characteristics of formative assessment in a way that serves as feedback in the teaching-learning process.

5.1. PROCEDURES

The evaluation must be inspired by the criteria of continuous evaluation (Learning Assesment Guidelines, LAG, art 3). However, in compliance with the regulations of the University of Alcalá, an alternative process of final evaluation is made available to the student in accordance with the Learning Assesment Guidelines as indicated in Article 10, students will have a period of fifteen days from the start of the course to request in writing to the Director of the Polytechnic School their intention to take the non-continuous evaluation model adducing the reasons that they deem convenient. The evaluation of the learning process of all students who do not apply for it or are denied it will be done, by default, according to the continuous assessment model. The student has two calls to pass the subject, one ordinary and one extraordinary.

To perform the assessment various tests and exercises are proposed, which are detailed below, together with the corresponding grading criteria.

According to current regulations and, since the experimental laboratory part is considered essential for the acquisition of the skills in this course, attendance at all laboratory sessions and passing lab practices will be considered compulsory in the assessment, both in the ordinary and in the extraordinary call (regulation of learning assessment processes approved by the Governing Council, September 30, 2021, Article 6, paragraph 4). For this reason, laboratory lectures are common and essential in both types of assessment: continuous and non-continuous.

5.2. EVALUATION

ASSESSMENT CRITERIA

The objective of the assessment process is to analyse what competences and skills the student has acquired and to what degree. The tests and procedures detailed next are presented in order to evaluate

the assessment criteria that are detailed below, related to learning outcomes:

CE1: Conceptually and correctly solve design problems in advanced digital electronic circuits: modelling, simulation, synthesis and verification, applying current design methodologies.

CE2: Apply the different theory chapters to solve in a creative and original way the proposed exercises.

CE3: Present and defend in a clear and reasoned manner their proposals for the resolution of the proposed exercises.

CE4: Implement in practice circuits that provide a solution to the proposed exercises, integrating the knowledge acquired on hardware description languages and making use of the bibliographic resources and computer tools.

CE5: Generate correctly written, clear and precise documentation about the work done in the laboratory.

Ordinary call

Continuous assessment

1. Carry out the different assessment tests that are established throughout the course.
2. Develop laboratory practices, of compulsory attendance.
3. Carry out a global test with several questions (analysis and/or synthesis) referring to specific aspects covered by the theory lectures, exercises and laboratory.

Final assessment

Students who choose the final evaluation must pass a final test with the following contents:

1. Theoretical-practical test, which will comprehensively cover the contents of all the topics from the theory, exercises classes and laboratory.
2. Practical laboratory tests, which will cover the objectives programmed in the corresponding part of the course. Note that attending these practical lab lectures is also compulsory in the final assessment.

Extraordinary call

Continuous assessment

For students who, having participated in the continuous assessment process, have not passed the course satisfactorily, the extraordinary call will consist of:

1. Theoretical-practical test, which will comprehensively cover the contents of all the topics from the theory, exercises classes and laboratory.
2. Practical laboratory test, which will cover the objectives programmed in the corresponding part of the subject, for those students who, having been evaluated of the practices in the ordinary call, have not passed them. The practical mark of the ordinary call may be kept for the extraordinary call if the student has satisfactorily passed the evaluation of the competences related to them.

Final assessment

The grading procedure for this type of assessment will be the same in both calls.

GRADING INSTRUMENTS

This section specifies the assessment instruments that will be applied to each of the assessment criteria.

- **PEI:** An intermediate evaluation test of the contents from blocks 1 and 2, which will consist of

several questions with a similar duration to those of the final exam.

- **PL1:** Guided practice on the study of the internal architecture of FPGAs, the development card and the tools to be used.
- **PL2:** Practice on a free digital electronic design of medium complexity. It will cover the theoretical blocks 1 to 3.
- **PC:** A global test with several problems (analysis and/or synthesis) referring to specific aspects covered by the theory and exercises classes, and a question related to the laboratory.
- **PEF:** Final test for the final assessment with several questions (analysis and/or synthesis) referring to specific aspects covered by the theory classes, exercises and laboratory.

GRADING CRITERIA

A. Ordinary call

Continuous assessment. The relationship between the criteria, instruments and grading is as follows:

Skill	Learning Outcomes	Grading criteria	Grading instrument	Grading weight
TR2, TR8, CSE5, CSE7	RA1, RA3, RA4	CE1, CE2, CE3	PEI	25%
TR2, TR8, CSE3	RA2, RA3	CE1, CE2, CE3, CE5	PL1	5%
TR2, TR8, CSE1, CSE3, CSE5, CSE7	RA2, RA3, RA4	CE4, CE5	PL2	30%
TR2, TR8, CSE1, CSE2, CSE3, CSE5, CSE7	RA1, RA3, RA4, RA5, RA6, RA7	CE1, CE2, CE3	PC	40%

Students will be considered to have passed the course (proving the acquisition of theoretical-practical skills) according to the continuous assessment if the following requirements are met:

- They have carried out the intermediate evaluation tests (PEI).
- They have satisfactorily passed the assessment of skills related to laboratory practices. It will be understood that a student acquires these skills satisfactorily if he/she attends the laboratory and completes all the practices, obtaining a grade in that part greater than or equal to 5 out of 10 marks.
- They have satisfactorily passed the assessment of the skills related to all the theoretical tests. It will be understood that a student acquires these skills satisfactorily if their grade in this part is equal to or higher than 45% of the maximum grade obtainable ($PEI \times 0.25 + PC \times 0.4 \geq 2.9$ out of 10 marks).
- The final weighted grade of all the continuous assessment tests defined turns out to be equal to or greater than 5 out of 10 marks ($PEI \times 0.25 + PC \times 0.4 + PL \times 0.35 \geq 5.0$).

The student who follows the continuous assessment model will be considered as not presented in the ordinary call when he/she does not carry out the global test (PC).

Note: PEI= Intermediate assessment test; PC= Global test; PL= Lab practices.

Final assessment. The criteria, instruments and grading are the following:

Skill	Learning Outcomes	Grading criteria	Grading instrument	Grading weight
TR2, TR8, CSE1, CSE2, CSE3, CSE5, CSE7	RA1, RA3, RA4, RA5, RA6, RA7	CE1, CE2, CE3	PEF	65%
TR2, TR8, CSE1, CSE3, CSE5, CSE7	RA2, RA3	CE1, CE2, CE3, CE4, CE5	PL	35%

Students will be considered to have passed the subject if the following requirements are met:

- The weighted final grade of all Final assessment tests turns out to be equal to or greater than 5 out of 10 points.
- The assessment of skills related to laboratory practices has been satisfactorily passed. It will be understood that a student acquires these skills satisfactorily if he/she obtains a grade in that part greater than or equal to 5 out of 10 points.
- The assessment of the skills related to the theoretical test (PEF) has been successfully passed. It will be understood that a student acquires these skills satisfactorily, if their grading is equal to or greater than 50% of the maximum grade obtainable.

B. Extraordinary call

Continuous assessment. For students who, having participated in the continuous assessment process, have not passed the course satisfactorily, the extraordinary call will consist of:

Skill	Learning Outcomes	Grading criteria	Grading instrument	Grading weight
TR2, TR8, CSE1, CSE2, CSE3, CSE5, CSE7	RA1, RA3, RA4, RA5, RA6, RA7	CE1, CE2, CE3	PEF	65%
TR2, TR8, CSE1, CSE3, CSE5, CSE7	RA2, RA3	CE1, CE2, CE3, CE4, CE5	PL	35%

Students, who do not obtain a final overall grade higher than 5 out of 10 marks in the ordinary call, may, if desired, keep the complete theory part (PEF=PEI+PC) for the extraordinary call. That is, it is possible to keep the theory grade or the laboratory one independently. This call will have the same procedure and grading criteria described for the ordinary call for them.

Final assessment. The grading criteria is the same for both calls.

CHARACTERISTICS OF CONTINUOUS ASSESSMENT TESTS

The objective of the intermediate tests is not to fragment the final exam or the grade into individual partials but:

- Allow the student to know, throughout the learning process, with a real and objective test, what the assessment and grading criteria are, which were presented at the beginning of the course.
- Allow the student to evaluate at the end of each block the learning process that has been carried out, as well as the acquired competences and skills.
- Provide teaching staff with a feedback about the quality of the implementation and development of the course.
- The student will receive detailed information about the results of the intermediate tests so that he/she can evaluate the learning process, detect the gaps and solve any possible issue.
- The intermediate tests do not release any chapter for the final exam, since the objective of this is to evaluate the global acquisition of skills in the course. One of these skills, of vital importance in this course, is the ability to apply and relate all the knowledge acquired in a coordinated way towards the resolution of an exercise.

- Any student, who is not satisfied with their grading in the intermediate tests, can discard this grade and carry out the corresponding part in the final global test. In this way, the intermediate tests can be, in an effective way, a tool of self-assessment and improvement of the learning process, without implying a drawback for those students who do not satisfactorily pass them.

6. BIBLIOGRAPHY

6.1. Basic Bibliography

- Documentation generated by the teaching staff for the course, which will be provided to students directly, or posted on the course website.
- Selected websites related to the content of the module.
- J. M. Rabaey. “Digital Integrated Circuits: A Design Perspective”, 2nd edition. ed. Prentice-Hall, 2003.
- L. Terés, Y. Torroja, S. Olcoz y E. Villar. “VHDL Lenguaje estándar de diseño electrónico”, ed. McGrawHill, 1998.
- Fernando Pardo y José A. Boluda.” VHDL. Lenguaje para síntesis y modelado de circuitos”, ed. RAMA.1999.
- R. L. Geiger, P. E. Allen and N. R. Strader. “VLSI design techniques for analogue and digital circuits”, ed. McGraw-Hill, 1989.
- N. Jha and S. Gupta. “Testing of digital systems”, ed. Cambridge University Press, 2003.
- S. M. Sze and M.-K. Lee. "Semiconductor Devices (Physics and Technology)”, ed. Wiley, 1st edition (1985) y 2nd edition (2002).

6.2. Additional Bibliography

- S. Alonso, E. Soto y S. Fernández. “Diseño de Sistemas Digitales con VHDL”, ed. Thomson, 2002.
- T. H. Lee. “The design of CMOS Radio-frequency Integrated Circuits”, Cambridge University Press, Cambridge, 1998.
- D. Johns and K. Martin. “Analog Integrated Circuit Design”, John Wiley & Sons, Inc., New York, 1997.
- Peter J. Ashenden and Jim Lewis. “The designer’s guide to VHDL", Third edition, ed. 2008 Published by Morgan Kaufmann Publishers.
- Pong P. Chu. "RTL Hardware Design Using VHDL", John Wiley & Sons Inc., 2006.
- J. P. Deschamps. “Síntesis de circuitos digitales”, ed. Thomson, 2002.
- P. J. Ashender. “The VHDL Cookbook”, University of Adelaida, 1990.
- U. Meyer-Baese. Digital Signal Processing with Field Programmable Gate Arrays, Springer, 2007.
- I. A. Grout. “Integrated circuit test engineering”, ed. Springer-Verlag, 2006.
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- K. R. Laker and Willy W. M. C. Sansen. "Design of analog integrated circuits and systems", 1st edition, McGraw-Hill College, 1994.
- S. Franco. "Design with Operational Amplifiers and Analog Integrated Circuits", 2nd Edition, McGraw-Hill, 1998.

Disclosure Note

During the evaluation tests, the guidelines set out in the Regulations establishing the Rules of Coexistence of the University of Alcalá must be followed, as well as the possible implications of the irregularities committed during said tests, including the consequences for committing academic fraud according to the Regulation of Disciplinary Regime of the Students of the University of Alcalá.